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13. ABSTRACT (Maximum 200 words)

The project aimed at significant improvement of the III-nitride based epitaxial materials and device design and fabrication for high-power heterostructure field-effect transistors (HFETs). The key innovative approaches implemented in this program include novel pulsed atomic layer epitaxy (PALE) technique to grow the buffer layer with low defect density, improved epitaxial uniformity in multi-wafer MOCVD reactor, growing HFET wafers with the sheet resistance below 300 Ohm/square. Design improvements include double-heterostructure devices (DHFET) with InGaN electron confinement layer, insulated gate design using SiO2 gate insulator (MOSDHFETs) and innovative field-plate design. These new devices demonstrated high RF powers 15-20 W/mm at a drain bias of 50-65 V, and good parameter stability at 19 W/mm CW powers as confirmed by 100+ hours testing.

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Statement of the problem studied

The program focused on the most important unresolved problems that impede the incorporation of high-power nitride based heterostructure field-effect transistors (HFETs) technology into defense and commercial systems. These problems include:

1. Poor doping, thickness and composition uniformity of the HFET epitaxial layers over (2") substrates.
2. Poor reproducibility of epitaxial growths from run to run.
3. Lack of availability and epitaxial growth optimization over 4" substrates.
4. Aging effects and parameter degradation in AlGaN/GaN HFETs.
5. RF dispersion and current collapse in AlGaN/GaN HFETs high-power devices.

To overcome the above problems several innovative research approaches has been undertaken in the course of the program. The major research efforts have been aimed to:

- Develop innovative buffer-layer technology to mitigate substrate surface and bulk quality.
- Improve epitaxial uniformity in multi-wafer reactor to meet program goals.
- Scale-up growth process to 4-inch substrates.
- Incorporate double heterostructure epilayer designs for improved carrier confinement (***DHFET***)
- Improve the performance and stability via insulating gate (MOSDHFET) device design.
- Correlate material and device characteristics to study and optimize:

  Current collapse

  Long-term DC and RF power stability

Summary of the key achievements.

I. Uniformity and quality of epitaxial materials for HFET devices

Epitaxial barrier/ buffer layers quality is a key parameter controlling the DC and RF performance of the nitride based HFETs. The problem of growing the high quality materials arises mainly from significant lattice mismatch between the SiC substrate and GaN epitaxial layer as well as form the strain induced at the GaN - AlGaN interface.

A novel approach to radically improve the GaN buffer layer quality based on pulsed atomic layer epitaxy (PALE) further developed into more advanced Migration Enhanced MOCVD (MEMOCVD) technology was used. These new techniques resulted in significant improvement in the GaN crystalline quality.

GaN buffer layers grown by conventional MOCVD technique demonstrated the X-ray diffraction ω-scan with the HWFM of typically 550 sec. Novel pulsed epitaxial growth technique resulted in 330 sec line-width (PALE growth), which was further improved to obtain 230 sec line-width (MEMOCVD growth) in the course of the program. Excellent run-to-run uniformity of the XRD ω-scan line-width was achieved. For 15 sequential runs, the line-width deviation does not exceed 50 sec.

The pictures below illustrate the quality of MEOCVD grown 2", 3" and 4" HFET structures.

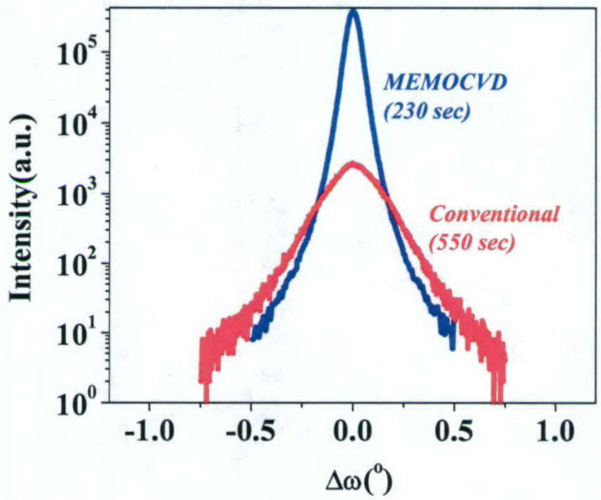

Figure 1. XRD omega scan of MEMOCVD grown AlN buffer

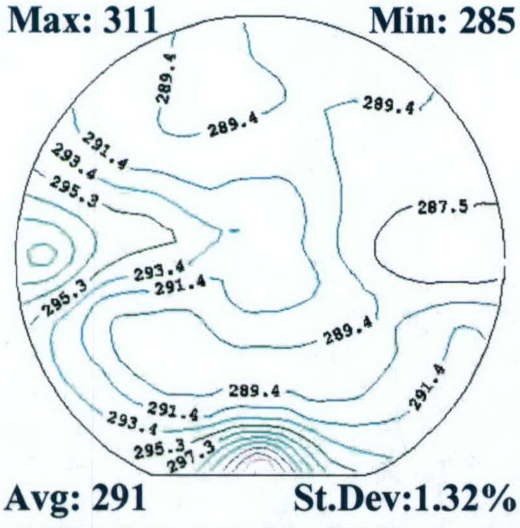

Figure 2. Resistivity map of the HFET structure on a 2" SiC wafer

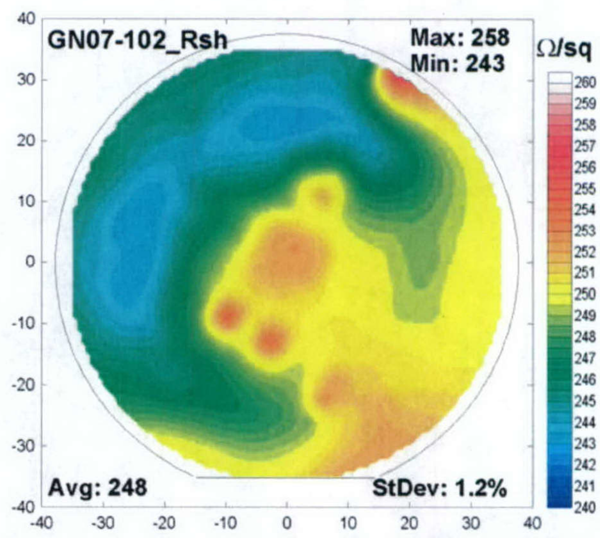

Figure 3. Resistivity map of the HFET structure on a 3" SiC wafer

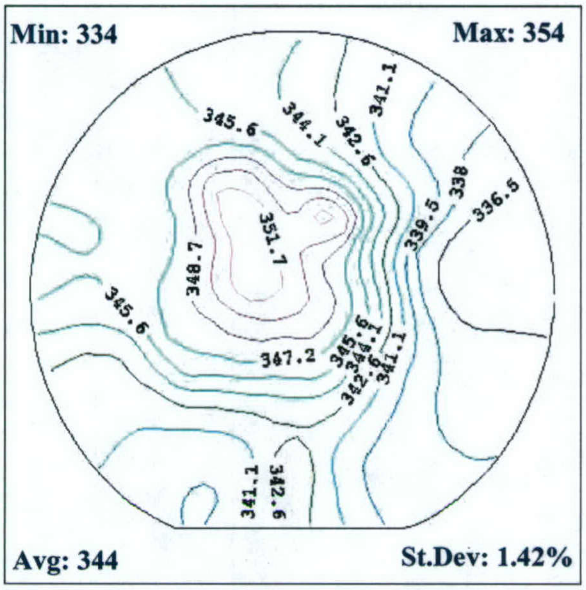

Figure 4. Resistivity map of the HFET structure on a 4" sapphire wafer

II. Insulated Gate MOSDHFET Device design

Gate leakage current in conventional HFETs is a major contributor to device instability and failure. The development of Metal-Oxide-Semiconductor Insulated gate HFETs (MOSHFETs) leads to the gate leakage currents four to six orders of magnitude lower than those of the HFETs (see Figure 5). The MOSHFETs has demonstrated a significant performance improvement as compared to conventional HFETs resulting in higher channel currents and RF powers. In the course of this study, we have carried out a comparative experimental evaluation of the HFET and MOSHFET lifetime at room and elevated temperatures. The room temperature MOSHFET stability lifetime as high in excess of 21,000 hours is estimated. The pronounced similarity of the mechanisms of device degradation and current collapse has been observed.

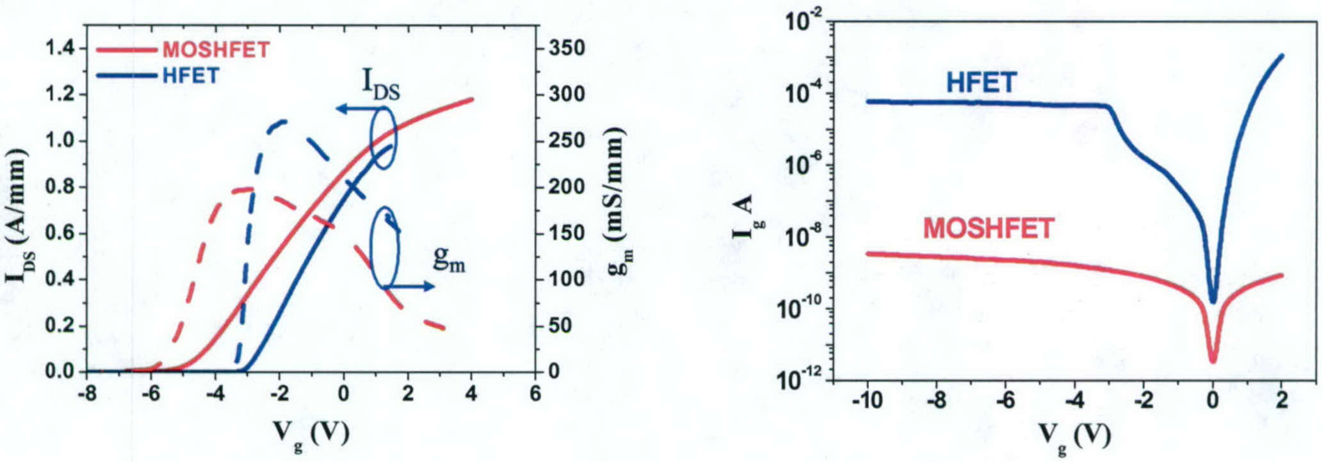

Figure 5. Comparative I-V characteristics of the sub-micron gate HFET and MOSHFET

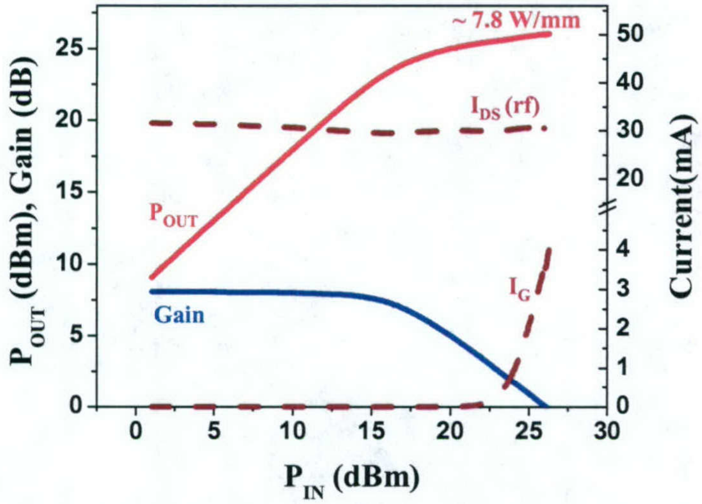

Figure 6. The effect of high input RF powers on the HFET gate leakage currents.

Figure 6 illustrates an increase in the DC components of the HFET gate current with the input RF powers. Note that the gate current direction corresponds to the forward currents in spite of the negative DC bias. When a Schottky gate FET operates under large input signal, the maximum peak gate voltage may cause forward currents through the gate leading to different degradation mechanisms, including tunnel and avalanche breakdown. Dynamic forward gate biasing becomes even more important in high-power high-voltage devices such as AlGaN/GaN HFETs.

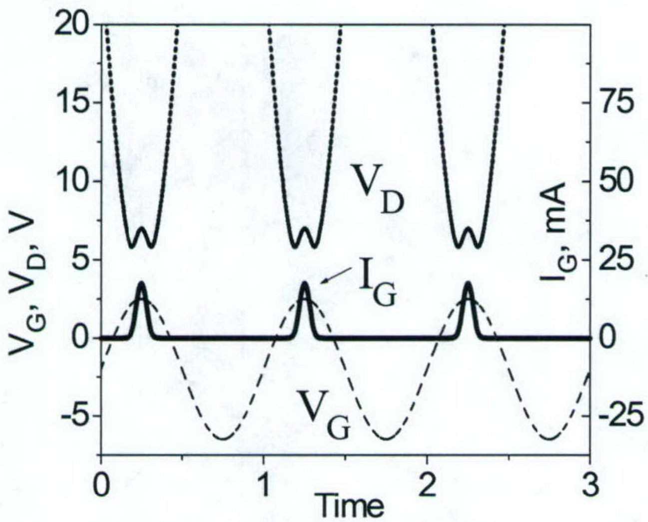

Figure 7. Aim-Spice simulations for the HFET gate voltage, drain voltage and gate current at 40 V drain bias and -2V gate bias. For the simulations, the model parameters were fitted to the experimental HFET data. The capacitive component of the gate current is not shown to simplify the waveforms.

As seen from Figure 7, the dynamic forward biasing coming from a large amplitude of the input signal causes up to 25 mA peak forward gate currents. We have found a strong correlation between RF power stability and an increases in the dynamic forward gate currents, as illustrated in Figure 8.

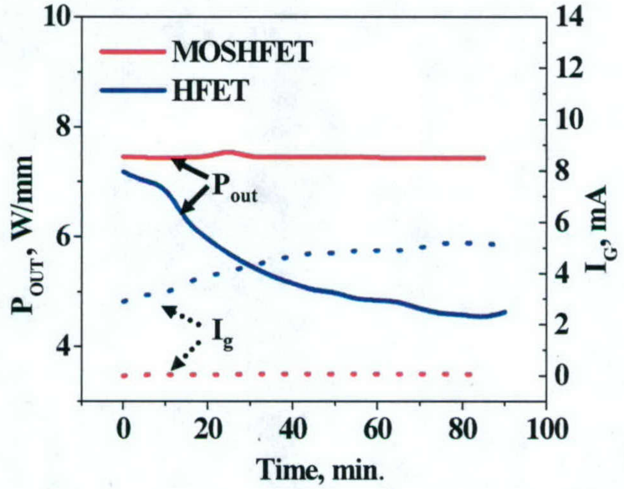

Figure 8. RF stability of the HFET and MOSHFET devices fabricated on the same SiC wafer.

III. Stable High-Power Field-Plated MOSDHFET.

Using a field-plate (FP) device design that was previously applied to GaAs HEMTs, several groups (NEC, UCSB, Cornell Univ., TriQuint et. al.) recently reported on HFETs with significantly improved RF-power performance, which they attributed to an increase in the breakdown voltage and a decrease in the current-collapse by the channel field reduction. They demonstrated microwave powers ranging from 10-W/mm at V_{ds} = 65 V to 30 W/mm at V_{DS}= 120 V. However, all the reported FP devices suffered from degradation at high RF power levels. As confirmed by several research groups including ours, the degradation mainly comes from the excessive gate current.

The MOSHFET design approach allows the application of high positive gate voltages thereby increasing the device peak currents. It also suppresses the gate leakage current. In the course fo current work, combining the MOSHFET design with a field-plate, we for the first time achieved a stable operation at 2 GHz for times in excess of 100 hours and at power densities as high as 19-W-mm (V_{ds} = 55 V). The extremely low leakage currents for our insulating gate device configuration enable us to achieve the long term stability in spite of the high power densities.

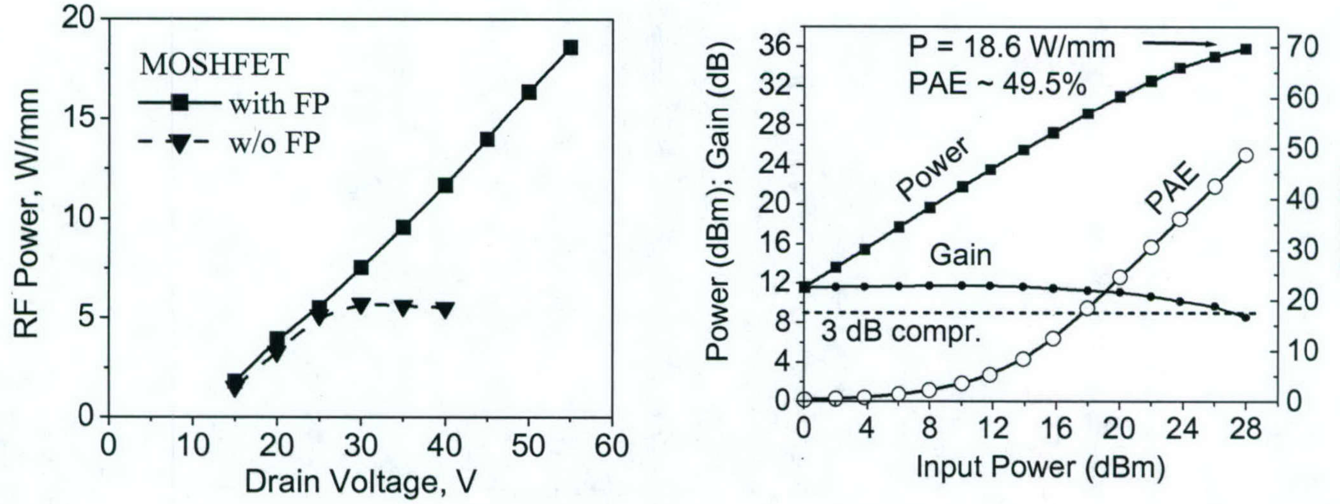

Figure 9. (a): Drain bias dependence of output RF power at 2 GHz for a MOSDHFET with and without field plate. (b): Power sweep at 2 GHz for 200 μm wide device. The device dimensions are: $L_{sd} = 6$ μm, $L_g = 1.1$ μm, $L_{FP} = 2.1$ μm with a 1.1 μm overlap with the gate.

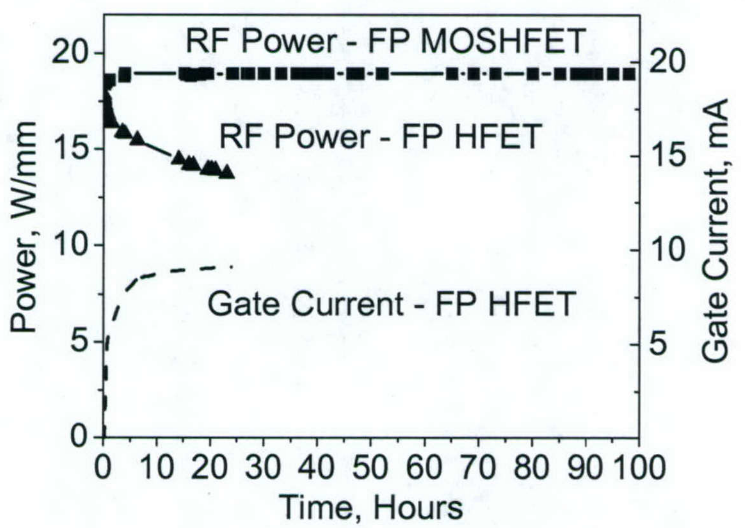

Figure 10. Output power at 2GHz for identical geometry field-plated MOSHFET and HFET as a function of time. The drain bias for both FP device types was 55 V. The right axis shows the time dependence of DC component of the HFET gate current. The current under the MOSHFET gate is too low to be shown and does not show any significant increase over the time.

IV. Conclusion.

By combining the innovative growth, device design and fabrication technique, in the course of this project we demonstrated the highest RF powers (close to 20 W/mm) at 55V drain bias, the highest Power-Voltage efficiency (0.36 W/V) and the first high-power stable performance at the power levels as high as ~20W/mm. We have also successfully demonstrated the technology scale-up to grow high-quality 3" and 4" HFET epitaxial structures..

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